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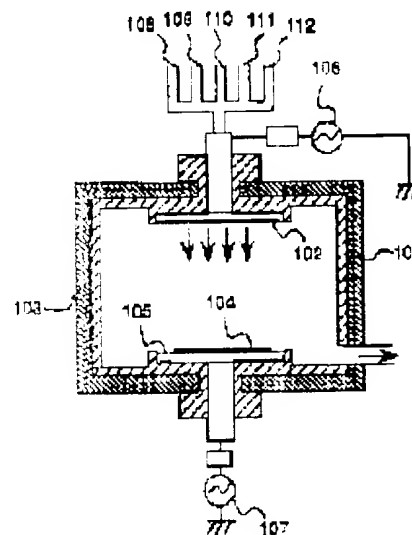
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(54) PLASMA CHEMICAL VAPOR DEPOSITION DEVICE, AND MANUFACTURE OF SEMICONDUCTOR DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To form a film with little plasma damage at low cost by providing a mechanism of forming an insulating film by generating plasma between parallel plate type of electrodes, in low pressure region, within a CVD reaction chamber.

SOLUTION: For a reaction chamber, the sidewall 101 of the CVD chamber is a conductor (aluminum, or the like), and the inwall is insulated with an insulator (alumina or the like) 103. Furthermore, this is a parallel board type of plasma CVD device where the peripheries of a gas supply head (upper electrode 120), which equalizes and supplies reaction gas, and a heating sample stage (lower electrode 105) are sealed with insulators, whereby the discharge between the electrode and the sidewall can be prevented. Furthermore, it becomes possible to discharge more stably at low pressure of 0.5 Torr or under by widening the interval between electrodes to 50mm.



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CLAIMS

[Claim 1]

[Claim 1] In a reaction chamber, it is 0.5 Torr. Plasma-chemistry vapor-growth equipment characterized by having the mechanism which parallel monotonous type inter-electrode is made to generate plasma, and forms an insulator layer in the following low voltage fields.

[Claim 2] An insulator is included around an electrode and it is 0.5 Torr. Plasma-chemistry vapor-growth equipment characterized by having the mechanism which parallel monotonous type inter-electrode is made to generate plasma, and forms an insulator layer in the following low voltage fields.

[Claim 3] A conductor shield is formed around an electrode and it is 0.5 Torr. Plasma-chemistry vapor-growth equipment characterized by having the mechanism which parallel monotonous type inter-electrode is made to generate plasma, and forms an insulator layer in the following low voltage fields.

[Claim 4] Plasma-chemistry vapor-growth equipment which has the mechanism in which RF power is impressed to an up electrode and the lower electrode which served both as the sample electrode holder in claims 1, 2, or 3, respectively.

[Claim 5] It sets to a claim 4 and is 13.56MHz to the aforementioned up electrode. Plasma-chemistry vapor-growth equipment which has the mechanism in which the above RF power is impressed.

[Claim 6] Plasma-chemistry vapor-growth equipment which has the mechanism in which RF power 50kHz or more is impressed to the aforementioned lower electrode, in a claim 5.

[Claim 7] Plasma-chemistry vapor-growth equipment which has the mechanism in which the first RF power 50kHz or more and two or more second positive pulse power are impressed to the aforementioned lower electrode, in a claim 6.

[Claim 8] The semiconductor device which has the mechanism in which impression of the RF power of the aforementioned up electrode is stopped after it impresses a RF to the lower electrode holding a substrate in claims 1, 2, 3, 4, 5, 6, or 7 after impressing a RF to the aforementioned up electrode, and stopping impression of the RF power of the aforementioned lower electrode.

[Claim 9] Plasma-chemistry vapor-growth equipment of a silicon oxide to which piping which introduces the gas containing Si, the gas containing oxygen or oxygen, inert gas, and a halogen or halogenation gas in claims 1, 2, 3, 4, 5, 6, 7, or 8 is connected.

[Claim 10] The aforementioned plasma-chemistry vapor-growth equipment of claims 1, 2, 3, 4, 5, 6, 7, 8, or 9 is used, and it is 0.5 Torr. The manufacture method of the semiconductor device which forms a silicon oxide by the plasma-chemistry vapor growth using the gas which contains Si in the following low voltage fields, and the gas containing oxygen or oxygen.

[Claim 11] The manufacture method of the semiconductor device which forms a silicon oxide by the plasma-chemistry vapor growth in a claim 10 using inert gas with the large atomic number from the gas containing Si, the gas containing oxygen or oxygen, argon, gas, or an argon.

[Claim 12] The manufacture method of a semiconductor device that the gas which contains Si in claims 10 or 11 is either the alkoxysilane which has an alkoxy group and Si-H combination, or a mono silane.

[Claim 13] The manufacture method of a semiconductor device that the gas which contains Si in a claim 12 is either trimethoxysilane or triethoxysilane.

[Claim 14] The manufacture method of the semiconductor device which is the silicon oxide in which the gas containing Si is the FUKOEO alkoxysilane or the FURORO alkoxide containing a fluorine, and the film to form contains a fluorine in claims 10 or 11.

[Claim 15] The manufacture method of a semiconductor device that the gas which contains Si in claims 10 or 11 is $\text{FSi}(\text{OCH}_3)_3$, $\text{FSi}(\text{OC}_2\text{H}_5)_3$, $\text{FSi}(\text{OC}_3\text{H}_7)_3$, $\text{FSiH}(\text{OCH}_3)_2$, $\text{FSiH}(\text{OC}_2\text{H}_5)_2$, $\text{FSiH}(\text{OC}_3\text{H}_7)_2$, SiH_2F_2 , or SiH_2F_2 .

[Claim 16] The manufacture method of a semiconductor device that the gas which contains Si in claims 10 or 11 is a tetraethyl orthochromate silicate.

[Claim 17] The manufacture method of the semiconductor device which forms a silicon oxide on this film by the chemistry gaseous-phase depositing method for having used the applying method or ozone after forming a plasma silicon oxide by the manufacture method of the aforementioned semiconductor device of claims 10, 11, 12, 13, 14, 15, or 16.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[The technical field to which invention belongs] this invention relates to the manufacture method of the chemical-vapor-deposition equipment used for the insulator layer formation during the metal wiring in a multilayer interconnection, and a semiconductor device.

[0002]

[Description of the Prior Art] The Si oxide-film forming method using three typical plasma as a method of forming the insulator layer for multilayer interconnections is learned.

[0003] The first, it is the method currently called parallel monotonous type plasma CVD method, and using plasma CVD equipment with the CVD room side attachment wall and parallel monotonous type electrode of aluminum, it is the pressure field of 2 - 10 Torr, and film formation is performed under the so-called ***** conditions 10mm or less. The thing of a single cycle method which impresses the RF power of 13.56 MHz from an up electrode, and the thing of a 2 cycle excitation method which impresses RF (50kHz - 13.56MHz) power also to a substrate side are known. As for Si source, it is common to use a tetraethyl orthochromatic silicate (TEOS).

[0004] The second is the bias spatter method of Si oxide film. A pressure arranges a substrate for the target of a quartz to another electrode at one electrode side in the chamber kept at about 5-30 mTorr, generates plasma, carries out sputtering of the quartz of a target, and makes it deposit on a substrate by this method. While impressing RF power to the up electrode at this time, RF power was impressed in order to improve embedded nature also to a lower electrode.

[0005] The third is a bias impression high-density plasma CVD method represented by Bias efficient consumer response. If Bias efficient consumer response is explained to an example, a mono silane and oxygen are introduced into a CVD room, and it maintains at the constant pressure of about 10 mTorr, and is 2.45GHz. Microwave is impressed. The reaction chamber is equipped with the magnet, the electron cyclotron resonance was used, and the method which forms high-density plasma is taken. In order to prepare the covering configuration of the level difference section, in a substrate lateral electrode, it is 13.56MHz RF power is impressed.

[0006]

[Problem(s) to be Solved by the Invention] Such above-mentioned conventional technology is holding the next technical problem as a method of forming a semiconductor integrated circuit which is future and which turns minutely.

[0007] First, although a tetraethyl orthochromatic silicate and oxygen are used by the parallel monotonous type plasma CVD method, in connection with the densification of a multilayer interconnection, an aspect ratio (interval of the height/wiring of wiring) becomes high, and it is 0.3 micrometers. To the insulator layer demanded by subsequent detailed devices, level difference covering nature, a flattening property, hygroscopicity, and water resistance are mentioned as a technical problem.

[0008] Next, by the bias spatter method, having been as small as about per hour two sheets, and the throughput's having been small and the silicon oxide by which the spatter was carried out further adhered in the chamber, and it did not become the mainstream method of production that there was much particle in it not being suitable for composition control of a film like CVD, that the setting window of the bias conditions which acquire the shape of proper flush type is small, by having not prepared the cleaning mechanism, etc. [of membrane formation speed]

[0009] Next, the bias impression high-density plasma CVD method represented by bias efficient consumer response-CVD is holding flattening of the covering configuration of the triangle on the improvement in a throughput, the improvement in an operating ratio of the deposition process of equipment, production cost reduction, and a pattern, and the technical problem of suppression of a plasma damage on the membranous uniform disposition shown below.

[0010] First, the present level about the uniform disposition top of the membranous quality of the formed film has large dispersion in the etch rate to HF solution, when membranes are formed on the diameter of 6 inches, or a 8 inches substrate, and it is over 15%. You have to make this into 5% or less. This originates in formation of a uniform magnetic field being difficult. At this time, big dispersion also at membrane formation speed is seen. Equipment will become expensive if many things are equipped in order to raise the homogeneity of a magnetic field. The present bias efficient consumer response-CVD system is a price more than the double precision of equipment conventionally.

[0011] Moreover, it is necessary to decrease also about particle. This is because film formation is performed, while a mono silane performs sputtering under that it is a reactant high material and deep bias. Although prolonged cleaning was performed and this

particle reduction is tried, it is the big technical problem which should still be coped with. Since bias was impressed and the sputtering effect is used positively, a triangular covering configuration is formed on a pattern, a chemical mechanical-polishing (CMP) method must be applied for flattening, and this has also become one of the obstacles of cost reduction.

[0012] Parallel monotonous type plasma CVD equipment is used for this invention, and it is 0.5 micrometers. It is made to the detailed slot of a high aspect ratio for the purpose of the thing which performs film formation which performs film formation of a covering configuration without an overhang, and which has the outstanding water resistance which prevents transparency of moisture and for which few film formation of a plasma damage is performed at low cost.

[Means for Solving the Problem] In addition to electric discharge of an up electrode, the technical problem that film formation of the covering configuration which do not have an overhang using simple parallel monotonous type plasma CVD equipment be performed apply RF power 50kHz or more also to the lower electrode which served as the substrate electrode holder, or raise the insulation of an electrode and a side attachment wall, and can solve it by acquire the plasma stabilized by the low-pressure area (below 0.5 Torr) in parallel monotonous type inter-electrode.

[0014] The technical problem that film formation which has the outstanding water resistance which prevents transparency of moisture is performed is Si-H to the silicon source. It is solvable by using the alkoxy silane which has combination

[0015] The technical problem that few film formation of a plasma damage is performed is solvable by impressing RF power to the lower electrode holding a substrate, only while impressing RF power to an up electrode.

[0016] By arranging an insulator to the wall of a CVD reaction chamber, or installing a shield near the electrode, the unusual electric discharge which causes the instability in a low voltage field is prevented, and it is 0.5. If the plasma stabilized in inter-electrode in the low voltage below 1 Torr is formed, by making it low voltage, the average free process of ion will become large in inverse proportion to a pressure, and its vertical component which carries out incidence to a substrate will increase. Moreover, since the energy of the ion accelerated by the electric field by the side of a lower electrode increases and the effect of sputtering of this ion increases, it has the operation it is made not to form an overhang in the covering configuration in the level difference section.

[0017] Moreover, when the alkoxy silane which has Si-H combination is used for the silicon source, an Si-H basis can be made to contain in a film, as soon as it reduces the hydroxyl group in the film formed by the plasma CVD method, and it has operation that the precise film which prevents that moisture penetrates the inside of a film is obtained.

[0018] Moreover, while forming plasma, in order to spread gradually the charge by the self-bias produced in the lower electrode and to make it neutralize, impressing RF power to the lower electrode holding a substrate, only while impressing RF power to an up electrode acts so that the damage of plasma may be suppressed.

[0019]

[Embodiments of the Invention] The CVD room of one example of the CVD system of this invention is shown in drawing 1.

Composition of a reaction chamber was taken as the structure where are ***** (aluminum etc.) and the CVD room side attachment wall 101 insulates the wall with insulators (alumina etc.) 103. Furthermore, the circumference of the up (a gas supply head-cum-) electrode 102 which makes reactant gas uniform and supplies it, and the lower (a heating sample base-cum-) electrode 105 was also shielded with the insulator. The 2 cycle excitation CVD which impresses a RF (13.56MHz) to the up electrode 102, and impresses a RF generator (400kHz) to the lower electrode 105 was used for the plasma generating method.

[0020] An example of the electric discharge state by the electrode spacing and membrane formation pressure of this equipment which are parallel monotonous type plasma CVD equipment is shown in drawing 2. The ***** method was used for the conventional parallel monotonous type plasma oxidation film CVD system by the high-tension side (1 or more Torr) in order to enlarge membrane formation speed (field of one in drawing 2). However, in this field, the sputtering effect is insufficient and an overhang is looked at by the deposited oxide film. Since the average free process of the molecule in plasma is extremely small, this reason is for colliding with other molecules, before ion is fully accelerated. For example, the average free process of the molecule in the plasma in 4 Torr is about 0.1mm. It is the following. Since an average free process is proportional to the inverse number of a pressure in order to use the sputtering effect effectively, it is required to acquire the plasma stabilized in the large low voltage (1 or less Torr) of the average free process of ion (field of two in drawing 2). Since inter-electrode molecularity will increase if an electrode spacing is made large, also in the low-tension side, a stable electric discharge field exists from the conventional pressure.

[0021] When the pressure was simply lowered with conventional parallel monotonous type plasma equipment, plasma became unstable, came to discharge between the electrode and the side attachment wall soon, and stopped however, discharging well in inter-electrode. Then, the electrode circumference and the side attachment wall were insulated with the equipment of this invention. Thereby, electric discharge between an electrode and a side attachment wall was able to be prevented. Furthermore, they are 0.5 Torr(s) by extending an electrode spacing to 50mm. It became possible to discharge to stability more by the following low voltage.

[0022] About the frequency of the RF power impressed to an up electrode, it is 13.56MHz. Otherwise, 27MHz and 40MHz were examined. The electric discharge stabilized even if it used which frequency by adjusting matching of a matching box and resetting up the cut off frequency of a filter was maintained. There was a property [one / where frequency is higher] that a margin is large, to change of CVD conditions. This is because ionization degree becomes large with increase of frequency.

[0023] Moreover, it is 0.5-4mm near the electrode as one means by which I accept it in order to form the stable electric discharge in low voltage. The method which arranges the shield of ground potential about a gap was also examined. This method was also

effective in the stable electric discharge in low voltage.

[0024] Next, the membrane formation method is explained. It can mix with the gas which contains oxygen or oxygen using the material (TEFORO alkoxide) containing a silicon alkoxide or fluorines, such as a tetraethyl ortho silicate (henceforth, TEOS), and a trimethoxy silicate (henceforth, TMS) which contains Si-H in liquid material, a TOKI-TOKISHI silicate (henceforth, TTS), to reactant gas, and a silicon oxide can be deposited by the plasma CVD method. Moreover, by cleaning of a CVD room, it is CF₄. A reaction with the gas containing fluorine system gas, such as C₂F₆, removes the sediment of an electrode and a reaction chamber wall.

[0025] Next, an example is explained based on the example which formed the silicon oxide using TMS. The oxygen flow rate dependency of the membrane formation speed in the case of TMS was shown in drawing 3. It is 200 nm/min when an oxygen flow rate is set as 100 or more sccm. It turns out that the above membrane formation speed is obtained. In consideration of the membrane examination result described later, typical membrane formation conditions were defined, as shown in Table 1. [0026] The bottom of these conditions -- membrane formation speed -- about 200 nm/min (the case where 500nm is deposited) -- wafer conveyance 1 minute, flow rate and pressure regulation 0.5 minutes, and membrane formation time 2.5 minutes -- per [40 -- about 1 sheet a part -- it is. Moreover, cleaning takes 2 minutes and the processing time per sheet of membrane formation/cleaning process is 6.0. Processing of about ten per hour is possible at a part. Furthermore, in two or more sheet processor, processing of about about 25 per hour is possible (when the number of reaction chambers is three).

[0027]

[Table 1]

表1 プラズマ SiO₂の形成条件

Plasma CVD	DFP-TMS
Temperature (°C)	360 °C
Pressure (Torr)	0.1 Torr
Bubbler -N ₂	80 sccm (5°C)
O ₂	100 sccm
Carrier -N ₂	120 sccm
Ar	50 sccm
RF Power	300 W (13.56 MHz)
Bias Power	300 W (400 kHz)
Electrode Gap	20 mm

[0028] Next, the bias power dependency over level difference covering nature (coverage) is shown in drawing 4. This situation was shown in drawing 4. The order taper was not checked in 4Torr(s) of the pressure at the time of the conventional membrane formation. If the pressure is made into low voltage, they are about 0.5 Torr(s). The inclination for overhangs to decrease in number was accepted from the neighborhood 0.1 Torr. The then remarkable bias power dependency was accepted. Coverage is displayed with the tilt angle of the formed oxide film (drawing 4 (a)). From the 200W neighborhood, with the increase in bias power, the tilt angle of an oxide film turned into a wide angle of 90 degrees or more, and showed the order taper configuration theta became the inclination to ***** to constant value, more than by 400W (drawing 4 (b)). In the conventional 4Torr(s), since an order taper is not checked, having reduced the pressure and having enlarged the average free process and the effect by both in which the electric field which impress bias and accelerate ion near a substrate were formed have shown up. The pressures which show the same tilt angle when Ar is added are 0.2Torr(s). It shifted to the forge-fire high-tension side. This is considered to be based on the shock effect of the increase in plasma density, and Ar ion.

[0029] The bias stop-time dependency of the isolation voltage of a plasma silicon oxide is shown in drawing 5. The plasma oxidation film of 100nm of thickness was deposited on the low resistance silicon substrate, and the MOS diode in which square of two or more 1mm aluminum electrodes were formed was used for the sample. The vertical axis of drawing 5 is isolation voltage, and a leakage current is 1microA/cm². They are the electric field when reaching. A horizontal axis is the bias halt timing time at the time of formation of a plasma silicon oxide, and shows the value which subtracted the stopping time of RF power of an up electrode from the stopping time of RF power of a lower electrode. Negative time means having stopped RF power of an up electrode, after stopping RF power of a lower electrode.

[0030] When RF power of an up electrode is stopped after stopping RF power of a lower electrode as shown in drawing, it turns out that high pressure-proofing is maintained. This is for suppressing the charge of a blocking capacitor being spread and being charged in a substrate, and preventing dielectric breakdown, when a RF is stopped previously. In this invention, reactant gas is supplied to a reaction chamber, and low frequency is impressed a RF and impressed continuously in the place where the pressure

became fixed. Moreover, after stopping low frequency (bias) previously just before a membrane formation end (3 - 5 seconds before), the RF was stopped at the time of a membrane formation end.

[0031] Moreover, positive pulse power was impressed with the 400kHz RF power of a substrate lateral electrode. In pulse width, pulse height made 40V and the number of times of a repeat per second 200 times for 10⁶ns, according to this bias impression method, the electron with large mobility was drawn near to a substrate front face out of plasma as an effect of a pulse, electrification of a substrate front face could be made small, and the thing which is 10 conventional minutes and which is small suppressed by one or less was checked in damage by the charge up.

[0032] Next, the film property of the plasma oxidation film which used as the raw material, the triethoxysilane formed with this equipment is explained. It is 0.5%HF to drawing 6. The oxygen flow rate dependency of the etch rate at the time of using solution is shown, the silicon thermal oxidation film at the time of using this etching condition -- 2.3 nm/min and a TEOS-plasma oxidation film -- 9.5 nm/min it was. By the triethoxysilane-plasma oxidation film, an etch rate also increases with the increase in an oxygen flow rate. Furthermore, the range of an etch rate is 2.3 - 4.9 nm/min. It is lower than the plasma silicon oxide using these (TEOS).

[0033] The silicon oxide formed with this equipment was a very precise film. The oxygen flow rate dependency over a refractive index is shown in drawing 7. The refractive index of a TEOS-plasma oxidation film decreases with the increase in an oxygen flow rate, and becomes high rapidly by 50 or less seems. It was a film with silicon a little more superfluous than a silicon thermal oxidation film.

[0034] The water resistance of the oxide film deposited on drawing 8 with this equipment is shown. An appraisal method is the pressure-cooker (PCT) method, and investigated the moisture transparency prevention nature of an oxide film. The evaluation sample was made into the structure which deposited 200nm of PSG films 802 on the substrate 801, and deposited further 200nm of plasma oxidation films 803 evaluated on it (a) (b) (c). Before and after PCT evaluating this sample (humidification examination), FT-IR (Fourier transform type infrared extinction spectrum) measurement was performed, and absorbance change of P=O combination of the 1320cm⁻¹ neighborhood was investigated. The conditions of a humidification examination were performed for 168 hours, pressure 2atm, the temperature of 121 degrees C, and 100% of humidity. By the conventional plasma TEOS film, when it is after membrane formation and PCT processing and compares, the absorbance of P=O combination is after PCT processing, and becomes small, and it is shown that moisture is penetrating the inside of the plasma film 803 even to the TEOS-plasma oxidation film. However, under these conditions, change of P=O combination is not seen but is excellent in the TEOS-plasma oxidation film deposited with this equipment at moisture transparency prevention nature compared with a plasma TEOS film.

[0035] The covering configuration of the plasma oxidation film of this invention is explained using drawing 9. Drawing 9 (a) is the configuration of the oxide film deposited with conventional plasma CVD equipment, and an overhang is seen to wiring 902. However, the oxide film by this invention becomes large compared with the oxide film (a) of the former. Opening 7 of the wiring 901 upper part 1 to wiring 902 in a POLITE eye taper configuration (b). Furthermore, it is also possible to embed between wiring completely by optimization of CVD conditions (c).

[0036] Drawing 10 is drawing having shown the ground dependency when depositing an O3-TEOS film (SiO₂ film which made ozone and TEOS react thermally and made them form) on a plasma silicon oxide. A ground dependency is the phenomenon (a) whose front face is ruined, when an O3-TEOS film is deposited on an insulator like a plasma oxidation film, and as a result, flattening of the level difference section was made difficult. However, on the plasma oxidation film by this invention, the ground dependency of an O3-TEOS film was not seen, but flattening was possible for it without the void in between wiring (b). Furthermore, it is possible by combining with CMP (chemical machinery polish) to obtain the outstanding flat nature (c). Moreover, instead of an O3-CVD film, even if it forms an application insulator layer (SOG) in piles, the same effect is acquired.

[0037] If the alkoxysilane which contains Si-H in the source gas of a silicon oxide is used, a high water resistance film can be formed, there will be little particle, and restrictions on the handling of a safety aspect will become less than a mono silane, and a production cost will decrease. Even if it does not impress extreme bias, there is an advantage that high rank difference covering nature is obtained.

[0038] Moreover, if TEOS is used for source gas, the precise silicon oxide of an order taper can be formed.

[0039] Although the explanation so far has followed the silicon oxide of a non dope, if it adds using the source gas containing F, the low dielectric constant film containing F can be formed into a film. Moreover, a silicon nitride can be formed if a plasma-chemistry vapor growth is performed using the gas and ammonia gas containing Si.

[0040]

[Effect of the invention] According to this invention, the high covering nature layer insulation film of the semiconductor device which has detailed wiring using simple parallel monotonous type equipment can be formed. Moreover, if alkoxysilane is used, while there will be less particle than a mono silane and the yield of a product will improve, the plant-and-equipment investment for security decreases. Moreover, since the film of high water resistance can be formed, a laminating can be carried out to films which were extremely excellent in embedded nature, such as an application glass membrane and an ozone CVD film, and it can use these -- a low cost -- more -- quantity -- a dense semiconductor device can be manufactured.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] The cross section showing the reaction chamber of the plasma CVD equipment of one example of this invention.

[Drawing 2] The electric discharge property view showing the relation between a reaction chamber pressure and an parallel plate electric differential.

[Drawing 3] The measurement view showing the relation between an oxygen flow rate and membrane formation speed.

[Drawing 4] Explanatory drawing showing correlation of bias power and level difference covering nature.

[Drawing 5] Explanatory drawing showing the relation between bias halt timing time and pressure-proofing.

[Drawing 6] The property view showing the oxygen flow rate at the time of the plasma silicon-oxide formation which shows one example of this invention, and the relation of an etch rate.

[Drawing 7] The property view showing the relation between the oxygen flow rate at the time of the plasma silicon-oxide formation which shows one example of this invention, and the refractive index of the formed film.

[Drawing 8] The cross section of a waterproof evaluation sample.

[Drawing 9] The property view of the level difference covering nature of a plasma silicon oxide showing one example of this invention.

[Drawing 10] Explanatory drawing of the process of layer insulation film formation which shows one example of this invention.

[Description of Notations]

901 --- Plasma silicon oxide, 902 --- A CVD silicon oxide, 903 --- Aluminum wiring, 904

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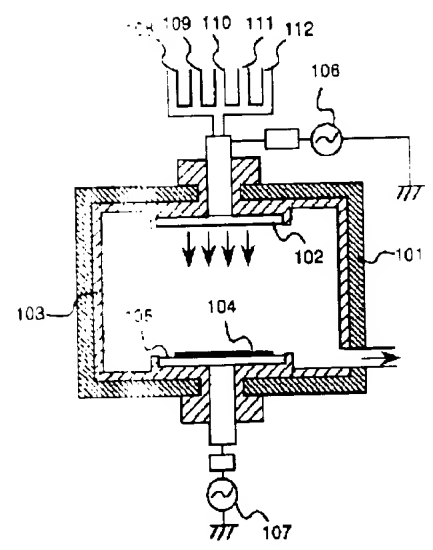
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DRAWINGS

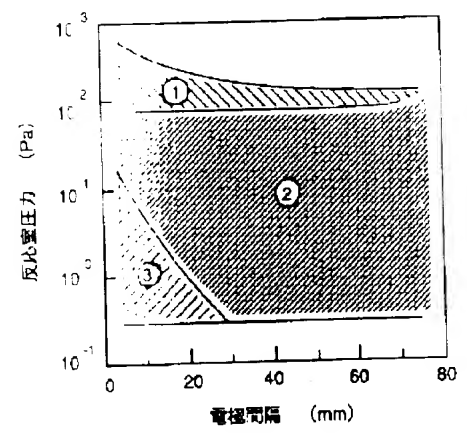
[Drawing 1]

図1



[Drawing 2]

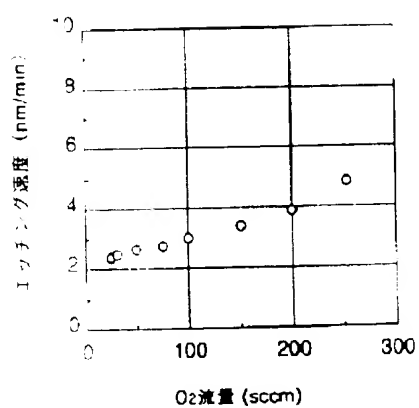
図2



- ① 電極間で安定放電する領域
- ② 電極間及びRF印加電極周囲で安定放電する領域
- ③ RF電極周辺のみで放電する領域

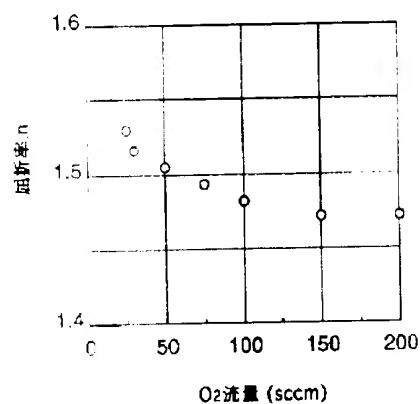
[Drawing 6]

図6



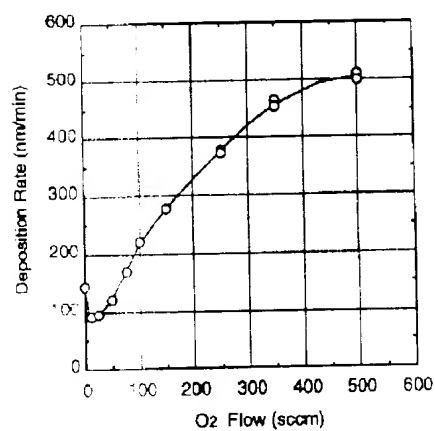
[Drawing 7]

図7



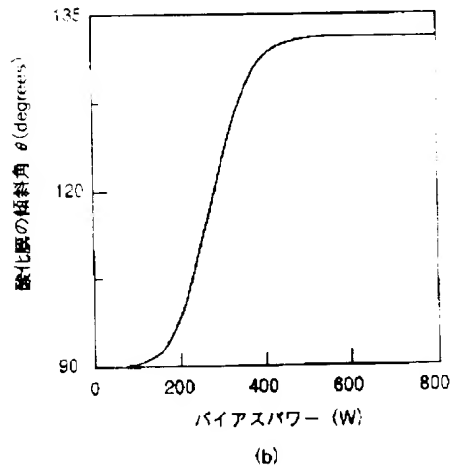
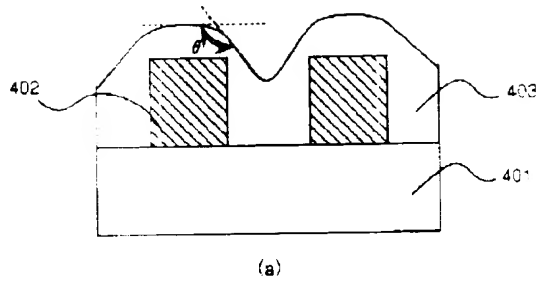
[Drawing 3]

図3



[Drawing 4]

図 4



[Drawing 2]

